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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/502,994	02/11/2000	Michael Mantor	11142	5992

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EXAMINER	
KLESS, GARY G	

ART UNIT	PAPER NUMBER
2672	

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Please find below and/or attached an Office communication concerning this application or proceeding.

NM

Office Action Summary	Application No.	Applicant(s)	
	09/502,994	MANTOR ET AL.	
	Examiner	Art Unit	
	Gary G. Kless	2672	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *18* is/are allowed.

6)☒ Claim(s) *1-10 and 13* is/are rejected.

7)☒ Claim(s) *11,12 and 14-17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Information Disclosure Statement

2 The listing of references in the specification is not a proper information disclosure statement. 37 CFR 1.98(b) requires a list of all patents, publications, or other information submitted for consideration by the Office, and MPEP § 609 A(1) states, "the list may not be incorporated into the specification but must be submitted in a separate paper." Therefore, unless the references have been cited by the examiner on form PTO-892, they have not been considered.

Claim Rejections - 35 U.S.C. 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 2, 5-10, and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang et al. U.S. Patent 5,831,640 in view of Schilling et al. U.S. Patent 6,236,405.

Regarding Claim 1, Wang et al. discloses a computer graphics processor system(col. 5, lines 15-16, 40-45, 33-37) having the capability of mapping texture(col. 6, lines 14-17) onto a three dimensional object in a scene being displayed(col. 5, lines 33-37), the system comprising:

(a) a texture address calculator(Fig. 3, element 220) for generating texel addresses for a list of primitives being processed(col. 7, lines 1-5, 12-15, 20-23).

(b) a texture cache controller(Fig. 3, element 250)for determining and requesting the necessary transfer of texels from said texture main memory(Fig. 3, element 102) addresses to said texture cache memory(Fig. 3, element 251)addresses ((col. 7, lines 55-58, col. 8, lines 2-5)(cache controller circuits and techniques are well known in the art)).

(c) a texture cache arbiter(Fig. 3, controller circuit 250) for scheduling controlling the actual transfer of texels from said texture main memory into the texture cache memory((col. 8, lines 2-5)(memory arbiters used to control fetching and transfer of data between memories are well known in the art and can be considered a part of a cache controller))

(d) a texture cache arbiter(250) for controlling the outputting of texels for each pixel to an interpolating filter(260) from the cache memory((col. 8, lines 30-33(cache controller circuit includes cache memory(Fig. 3)), col. 9, lines 60-63)(linear, bilinear, and trilinear filtering are well known in the art as interpolation filtering techniques)).

Wang et al. fails to disclose:

(e) a texture main memory containing an array of texels, each texel having an address and one of N identifiers.

(f) a texture cache memory having addresses partitioned into N banks, each bank containing texels transferred from said main memory that have the corresponding identifier.

However, Schilling et al. from a similar field of endeavor discloses limitations (e) and (f) as described above. Refer to Fig. 2 and col. 4, lines 15-19 for limitation (e) and col. 4, lines 15-19 for limitation(f). Fig. 2 shows an array of texels with each texel having one of four identifiers. Each 2x2 group af texels with identifiers 1, 2, 3, 4 are assigned to memory banks 1, 2, 3, and 4 respectively.

It would have been obvious to a person of ordinary skill in the art to incorporate the texture mapping system of Schilling et al. into the Wang et al. texture mapping system to provide a texture mapping system with high rendering speeds. Furthermore, such a texture mapping system would reduce the amount of data to be stored and accessed by a texture mapping system as suggested by Schilling et al.(col. 2, lines 1-4, 28-29).

Regarding Claim 2, Wang et al. fails to disclose the additional limitation to Claim 1 that the system further includes a texture addressing scheme for organizing the array of texels in main memory to group spatially related texels in one memory page.

However, Schilling et al. from a similar field of endeavor discloses a scheme for grouping spatially related texels(odd row/odd column, even row/odd column, odd row/even column, or even row/even column, Fig. 2) into dedicated memory banks corresponding to one of the aforementioned spatial relationships(col. 4, lines 13-17)

It would have been obvious to a person with ordinary skill in the art to combine the Schilling et al. texture mapping system, having a texel grouping feature, with the texture mapping system of Wang et al. to implement mipmapping in a rapid and cost efficient manner. Furthermore, texture would be rendered at higher speeds as suggested by Schilling et al(col.1, lines 63-67, col. 2, lines 7-9).

Regarding Claim 5, Wang et al. fails to disclose the additional limitation to Claim 2, wherein texture main memory contains an array of texels having addresses arranged in a plurality of even and odd numbered rows and columns, each texel having a cache memory identifier attached to each address in accordance with the following criteria: a first identifier assigned to texels with main memory addresses in both even rows and even columns; a second identifier assigned to texels with main memory addresses in both even rows and odd columns; a third identifier assigned to texels with main memory addresses in both odd rows and even columns; and a fourth identifier assigned to texels with main memory addresses in both odd rows and odd columns.

However, Schilling et al. from a similar field of endeavor discloses a method for assigning spatially related texels(odd row/odd column, even row/odd column, odd row/even column, or even row/even column spatial characteristics, Fig. 2) with a cache memory bank identifier each representing texels with addresses in main memory that have one of the aforementioned spatial characteristics(col. 4, lines 13-17).

It would have been obvious to a person with ordinary skill in the art to combine the Schilling et al. texture mapping system, having a memory bank identifier feature as described above, with the texture mapping system of Wang et al. to implement mipmapping in a rapid and cost efficient manner. Furthermore, texture would be rendered at higher speeds as suggested by Schilling et al(col.1, lines 63-67, col. 2, lines 7-9).

Regarding Claim 6, Wang et al. fails to disclose the additional limitation to Claim 5, wherein texture cache memory is arranged in four banks; each bank containing texels having one of four identifiers.

However, Schilling et al. from a similar field of endeavor discloses the additional limitation to Claim 5 as set forth above. Schilling et al. discloses(col. 4, lines 15-17) a method of arranging texture cache memory in four banks; each bank containing texels having one of four identifiers.

It would have been obvious to a person with ordinary skill in the art to combine the Schilling et al. texture mapping system, having a memory bank identifier method as described above, with the texture mapping system of Wang et al. The use of memory banks with identifiers enhances texture rendering speeds when combined with a texture mapping system as suggested by Schilling et al(col. 1, lines 65-67, lines 10-12).

Regarding Claim 7, Wang et al. fails to disclose the additional limitation to Claim 1, wherein texture main memory is organized into a plurality of texel blocks each having a cache memory identifier in accordance with the following criteria: each texel block consisting of at least one group of four contiguous texels(each having a per texel cache memory identifier); texture cache memory partitioned into rows corresponding to one of four block texel cache memory identifiers, each cache memory bank having at least one row corresponding to each of the four block texel cache memory identifiers.

However, Schilling et al. from a similar field of endeavor discloses the additional limitation to Claim 1 set forth above. Schilling et al. discloses a method of assigning block texel cache memory identifiers to groups of four contiguous texels(Fig. 2, level 1), each texel having a per texel memory

identifier(Fig 2, level 0). Schilling et al. discloses(col. 4, lines 13-18) a texture memory with four banks(banks 4, 5, 6, 7), each bank having a block texel memory identifier corresponding to a group of four contiguous texels.

It would have been obvious to a person with ordinary skill in the art to combine the Schilling et al. texture mapping system, utilizing a memory bank identifier method capable of storing texel blocks as described above, with the texture mapping system of Wang et al. The use of memory banks with texel block identifiers in the Schilling et al. texture mapping system as described above, improves data compression efficiency when combined with a texture mapping system as suggested by Schilling et al(col. 2, lines 1-4, 18-21).

Regarding Claim 8, Wang et al. fails to disclose the additional limitation to Claim 1 wherein said cache controller includes N stages.

However, Schilling et al. from a similar field of endeavor discloses the additional limitation to Claim 1 as set forth above. Schilling et al. discloses a cache controller(Fig. 8, element 812) capable of addressing 8 banks separately(col. 8, lines 60-67) through multiple stages of address lines(Fig. 8, (see lines from element 812 to element 822)).

It would have been obvious to a person with ordinary skill in the art to combine the Schilling et al. texture mapping system, utilizing memory banks managed by a multi-staged controller as described above, with the texture mapping system of Wang et al. The use of memory banks with a multi-staged controller in the Schilling et al. texture mapping system as described above, enhances data compression efficiency when combined with a texture mapping system as suggested by Schilling et al.(col. 2, lines 1-4, 18-21).

Regarding Claim 9, Wang et al. fails to disclose the additional limitation to Claim 7 wherein said cache controller includes four stages, each stage controlling the transfer of texels for one of the four block texel cache memory identifiers.

However, Schilling et al. from a similar field of endeavor discloses the additional limitation to Claim 7 as set forth above. Schilling et al. discloses a cache controller(Fig. 8, element 812) capable of addressing 4 banks (banks 4, 5, 6, 7- Fig. 8 element 810) separately(col. 8, lines 60-67) through multiple stages of address lines(Fig. 8, (see lines from element 812 to element 822)). Schilling also discloses that each stage of the controller guides the transfer of texels for one of the four block texel memory bank identifiers(col. 8, lines 60-67) by supplying each bank address decoder (Fig. 8, element 822) with an address and initiating a transfer.

It would have been obvious to a person with ordinary skill in the art to combine the Schilling et al. texture mapping system, utilizing memory banks managed by a multi-staged controller as described above, with the texture mapping system of Wang et al. The use of memory banks with a multi-staged controller in the Schilling et al. texture mapping system as described above, enhances texture rendering speeds when combined with a texture mapping system as suggested by Schilling et al(col.1, lines 65-67, col. 2, lines 9-12)

Regarding Claim 10, Wang et al. discloses a method wherein the cache controller transfers texture data at the main memory access granularity. According to Wang et al., the cache controller accesses and transfers texels(col. 7, lines 45-47) from main memory to the cache memory based on each texel(u, v) address of a texture map(col. 7,lines 10-17, lines 30-43).

Regarding Claim 13, Wang et al. fails to disclose the additional limitation to Claim 9 wherein the texture cache memory is a multi-ported cache memory enabling multiple texels to be retrieved in a single access.

However, Schilling et al. from a similar field of endeavor discloses the additional limitation to Claim 9 as set forth above. Schilling et al. discloses a method which allows two mipmap levels(multiple texels) to be retrieved in a single access(col. 4, lines 15-20) using eight independent memory banks each having a separate port for data transfer(Fig. 8, element 810).

It would have been obvious to a person with ordinary skill in the art to combine the Schilling et al. texture mapping system, utilizing multi-ported cache memory as described above, with the texture mapping system of Wang et al. The use of multi-ported cache memory in the Schilling et al. texture mapping system as described above, enhances data compression efficiency when combined with a texture mapping system as suggested by Schilling et al(col. 2, lines 1-4, 18-21).

5. Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang et al. in view of Schilling et al. as applied to Claims 1-2, 5-10, and 13 above, and further in view of Thayer et al., U.S. Patent 5,493,644.

Regarding Claim 3, Wang et al. in view of Schilling et al. as applied above fails to disclose the additional limitation to Claim 2, wherein the system further includes a span based polygon rasterization scheme so neighboring pixels of a primitive will be processed sequentially.

However, Thayer et al. discloses the additional limitation to Claim 2 as set forth above. Thayer et al. discloses a polygon span interpolator which incorporates a polygon rasterization system(col. 10 lines 43-47). Thayer et al. discloses a span based polygon rasterization scheme wherein polygon primitive span intersections with scan lines are located so that neighboring pixels of a primitive can be processed(col. 10, lines 49-54) sequentially along the span in the X direction.

It would have been obvious to a person with ordinary skill in the art to combine the polygon span interpolator system of Thayer et al. with the computer controlled graphics display system of Wang et al. as suggested by Thayer et al. (col. 4, lines 30-32) The combination described above maintains the processing speed and accuracy of scan converters while maintaining the cost effectiveness of a software scan conversion system as taught by Thayer et al(col. 3, lines 43-48).

Regarding Claim 4, Wang et al. discloses a system wherein the texture mapping capability includes storing pre-filtered textured maps at different resolutions and bilinear interpolation texture filtering. According to Wang et al., (col. 8, lines 30-37), the system stores bilinear filtered texture maps in a output FIFO memory device(Fig. 3, element 270). It is well known in the art that texture map resolution is determined by the filtering technique employed.

6. Claims 11, 12, 14-17 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. Claim 18 allowed.

Conclusion

8. Any inquiry concerning this communication from the examiner should be directed to Gary Kless whose telephone number is 703/305-3418. The examiner can normally be reached on Monday through Friday from 8:30 am to 5:00 pm.

gk

1/31/02

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